WHAT IS CLAIMED IS:

1. A method for storing a block of tiled data on first and second memory channels in an interleaved pattern comprising:

receiving a set of parameters that describe the block of data from a source;

determining a request address based on the parameters;

translating the request address to corresponding first and second tiled address channels based upon the parameters, further comprising:

determining, based upon selected tiled address bits, a corresponding tiled address for the first channel;

adding an offset to the first tiled address channel to produce a tiled address for the second channel; and

storing portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are accessible at the same time via first and second memory channels.

2. The method of claim 1, wherein the request address is directed to a X-major format tile and X-walk data request.

3. The method of claim 2, wherein the block of data is comprised of an aligned Hword.

4. The method of claim 3, wherein the first tiled address channel equals the request address and the second tiled address channel equals the request address + 16B responsive to:

(Tiled Address [8] = "0" AND Tiled Address [7] = "0") or

(Tiled Address [8] = "1" AND Tiled Address [7] = "1").

5. The method of claim 3, wherein the first tiled address channel equals the request address + 16B and the second tiled address channel equals the request address responsive to:

(Tiled Address [8] = "0" AND Tiled Address [7] = "1") or

(Tiled Address [8] = "1" AND Tiled Address [7] = "0").

6. The method of claim 1, wherein the request address is directed to a X-major format tile and Y-walk data request.

7. The method of claim 6, wherein the block of data is comprised of two adjacent Owords.

8. The method of claim 7, wherein the first tiled address channel equals the request address and the second tiled address channel equals the request address + 128 B responsive to:

(Tiled Address [4] = "0" AND Tiled Address [8] = "0") or
(Tiled Address [4] = "1" AND Tiled Address [8] = "1").

9. The method of claim 7, wherein the first tiled address channel equals the request address + 128K and the second tiled address channel equals the request address responsive to:

(Tiled Address [4] = "0" AND Tiled Address [8] = "1") or
(Tiled Address [4] = "1" AND Tiled Address [8] = "0").

10. The method of claim 1, wherein the request address is directed to a X-major format tile and Y-walk data request.

11. The method of claim 10, wherein the block of data is comprised of two Owords skipping one.

12. The method of claim 11, wherein the first tiled address channel equals the request address and the second tiled address channel equals the request address + 256 B responsive to:

(Tiled Address [4] = "0" AND Tiled Address [7] = "0") or

(Tiled Address [4] = "1" AND Tiled Address [7] = "1").

13. The method of claim 11, wherein the first tiled address channel equals the request address + 256 K and the second tiled address channel equals the request address responsive to:

(Tiled Address [4] = "0" AND Tiled Address [7] = "1") or

(Tiled Address [4] = "1" AND Tiled Address [7] = "0").

14. The method of claim 1, wherein the request address is directed to a Y-major format tile and x-walk data request.

15. The method of claim 14, wherein the block of data is comprised of an aligned Oword on a scan line.

16. The method of claim 15, wherein responsive to

(Tiled Address [5] = "0" AND Tiled Address [4] = "0") or

(Tiled Address [5] = "1" AND Tiled Address [4] = "1")

Channel 0 = Request Address

Qword (Tiled Address [3]) = Qword 0 of Source

Qword (Tiled Address [3]) = Not Used/Updated

Channel 1 = Request Address + 128B

Qword (Tiled Address [3]) = Qword 1 of Source

Qword (Tiled Address [3]) = Not Used/Updated.

17. The method of claim 15, wherein responsive to

(Tiled Address [5] = "0" AND Tiled Address [4] = "1") or

(Tiled Address [5] = "1" AND Tiled Address [4] = "0")

Channel 0 = Request Address + 128B

Qword (Tiled Address [3]) = Qword 1 of Source

Qword (Tiled Address [3]) = Not Used/Updated

Channel 1 = Request Address

Qword (Tiled Address [3]) = Qword 0 of Source

Qword (Tiled Address [3]) = Not Used/Updated.

18. The method of claim 1, wherein the request address is directed to a Y-major format tile and X-Y walk data request.

19. The method of claim 18, wherein the block of data is comprised of two Owords.

20. The method of claim 19, wherein the first tiled address channel equals the request address and the second tiled address channel equals the request address + 128 B responsive to:

(Tiled Address [5] = "0" AND Tiled Address [4] = "0") or

(Tiled Address [5] = "1" AND Tiled Address [4] = "1").

21. The method of claim 19, wherein the first tiled address channel equals the request address + 128 B and the second tiled address channel equals the request address responsive to:

(Tiled Address [5] = "0" AND Tiled Address [4] = "1") or

(Tiled Address [5] = "1" AND Tiled Address [4] = "0").

22. The method of claim 1, wherein the request address is directed to a Y-major format tile and Y walk data request.

23. The method of claim 22, wherein the block of data is comprised of a four adjacent Qwords.

24. The method of claim 23, wherein the first tiled address channel equals the request address and the second tiled address channel equals the request address + 16B responsive to:

(Tiled Address [7] = "0" AND Tiled Address [5] = "0") or

(Tiled Address [7] = "1" AND Tiled Address [5] = "1").

25. The method of claim 23, wherein the first tiled address channel equals the request address + 16B and the second tiled address channel equals the request address responsive to:

(Tiled Address [7] = "0" AND Tiled Address [5] = "1") or

(Tiled Address [7] = "1" AND Tiled Address [5] = "0").

26. The method of claim 1, further comprising:

determining first and second channel address bits based upon the tiled addresses for the first and second channel.

27. The method of claim 1, wherein the source includes a processor, wherein the processor stores and retrieves tiled data that includes a tiled representation of a video image.

28. The method of claim 27, wherein the processor further comprises an MPEG decoder, wherein the MPEG decoder stores and retrieves MPEG video data.

29. The method of claim 1, wherein the source includes a processor that generates graphics images that the processor stores and retrieves image data using the memory controller.

30. An apparatus for tiling a block of image data in an interleaved pattern among a first and second channel, comprising:

a processor;

a memory operably coupled to the processor, wherein the memory stores a mapping algorithm and a block of data, wherein when executed by the processor the mapping algorithm causes the processor to perform the function of:

determining, based upon selected tiled address bits, a corresponding tiled address for a first channel;

adding an offset to the first tiled address channel to produce a tiled address for a second channel; and

storing portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are accessible at the same time via first and second memory channels.

31. The apparatus of claim 30, wherein the data is stored in a X-major format tile.

32. The method of claim 30, wherein the data is stored in a Y-major format tile.

33. A machine readable medium having stored therein a plurality of machine readable instructions executable by a processor to store a block of tiled data on first and second memory channels in an interleaved pattern comprising:

instructions to receive a set of parameters that describe the block of data from a source;

instructions to determine a request address based on the parameters;

instructions to translate the request address to corresponding first and second tiled address channels based upon the parameters, further comprising:

instructions to determine, based upon selected tiled address bits, a corresponding tiled address for the first channel;

instructions to add an offset to the first tiled address channel to produce a tiled address for the second channel; and

instructions to store portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are accessible at the same time via first and second memory channels.

34. The machine readable medium of claim 30, wherein the request address is directed to a X-major format tile.

35. The machine readable medium of claim 30, wherein the request address is directed to a Y-major format tile.